

WHAT IS CLAIMED IS:

1. A coverage capture circuit for use with a general purpose performance counter ("GPPC") connected to a bus carrying N one-hot signals indicative of test coverage in a logic design, comprising:

an OR logic block for bit-wise ORing said N one-hot signals with an N -bit mask value stored in a register block, said OR logic block operating to generate an N -bit output; and

a Multiplexer (MUX) block operating to select said N -bit output from said OR logic block under control of at least one control signal, wherein said N -bit output is operable to be stored into said register block when selected by said MUX block.

2. The coverage capture circuit as recited in claim 1, wherein said OR logic block comprises N 2-input OR gates.

3. The coverage capture circuit as recited in claim 1, wherein said MUX block comprises N MUX elements, each for selecting a particular bit of said N -bit output.

4. The coverage capture circuit as recited in claim 1, wherein said MUX block comprises N MUX elements, each operating responsive to two control signals for selecting among up to four MUX inputs, including a particular bit of said N -bit output.

5. The coverage capture circuit as recited in claim 4, wherein one of said MUX inputs comprises a value stored in a control status register (CSR).

6. The coverage capture circuit as recited in claim 4, wherein one of said MUX inputs comprises said mask value stored in said register block.

7. The coverage capture circuit as recited in claim 4, wherein one of said MUX inputs comprises a fixed binary 0 value.

8. The coverage capture circuit as recited in claim 1, wherein each bit of said N -bit output stored in said register block comprises a binary 1 when a corresponding state in said logic design has been covered during a test.

9. A method of capturing test coverage information in a logic design, comprising:

generating N one-hot signals indicative of coverage of N states in said logic design under test;

bit-wise ORing said N one-hot signals with an N -bit mask value stored in a register block for generating an N -bit output; and

selecting said N -bit output by a Multiplexer (MUX) block operating under control of at least one control signal, wherein said N -bit output is operable to be stored into said register block when selected by said MUX block.

10. The method of capturing test coverage information in a logic design as recited in claim 9, wherein said N one-hot signals are operable to be encoded on an observability bus coupled to a general purpose performance counter ("GPPEC").

11. The method of capturing test coverage information in a logic design as recited in claim 9, wherein said bit-wise ORing operation is performed by an OR logic block comprising N 2-input OR gates.

12. The method of capturing test coverage information in a logic design as recited in claim 9, wherein said selecting of said N -bit output is performed by a MUX block comprising N MUX elements, each operating in response to two control signals for selecting among four MUX inputs, including a particular bit of said N -bit output.

13. The method of capturing test coverage information in a logic design as recited in claim 12, wherein one of said MUX inputs comprises a value stored in a control status register (CSR).

14. The method of capturing test coverage information in a logic design as recited in claim 12, wherein one of said MUX inputs comprises said mask value stored in said register block.

15. The method of capturing test coverage information in a logic design as recited in claim 12, wherein one of said MUX inputs comprises a fixed binary 0 value.

16. The method of capturing test coverage information in a logic design as recited in claim 12, wherein each bit of said N -bit output stored in said register block comprises a binary 1 when a corresponding state in said logic design has been covered during a test.

17. The method of capturing test coverage information in a logic design as recited in claim 9, wherein N is 80.

18. A system for capturing test coverage information in a logic design, comprising:

means for generating N one-hot signals indicative of coverage of N states in said logic design under test;

means for generating an N -bit output based on a logic operation between said N one-hot signals and an N -bit mask value stored in a register block; and

a Multiplexer (MUX) block operating to select said N -bit output under control of at least one control signal, wherein said N -bit output is operable to be stored into said register block when selected by said MUX block.

19. The system for capturing test coverage information in a logic design as recited in claim 18, wherein said N one-hot signals are operable to be encoded on an observability bus coupled to a general purpose performance counter ("GPPC").

20. The system for capturing test coverage information in a logic design as recited in claim 18, wherein said means for generating said N -bit output comprises an OR logic block that includes N 2-input OR gates for performing a bit-wise logic OR operation.

21. The system for capturing test coverage information in a logic design as recited in claim 18, wherein said MUX block comprises N MUX elements, each operating in response to two control signals for selecting among four MUX inputs, including a particular bit of said N -bit output.

22. The system for capturing test coverage information in a logic design as recited in claim 21, wherein one of said MUX inputs comprises a value stored in a control status register (CSR).

23. The system for capturing test coverage information in a logic design as recited in claim 21, wherein one of said MUX inputs comprises said mask value stored in said register block.

24. The system for capturing test coverage information in a logic design as recited in claim 21, wherein one of said MUX inputs comprises a fixed binary 0 value.

25. The system for capturing test coverage information in a logic design as recited in claim 21, wherein each bit of said N -bit output stored in said register block comprises a binary 1 when a corresponding state in said logic design has been covered during a test.

26. The system for capturing test coverage information in a logic design as recited in claim 18, wherein N is 80.